PATENT F0660/AMDP660US

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Date: 8-22-05 Himanshu S. Amin

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:	
Applicants(s): Bharath Rangarajan, *et al.*	Examiner: Richard A. Rosenberger
Serial No: 09/893,803	Art Unit: 2877
Filing Date: June 28, 2001	

Title: SYSTEM AND METHOD FOR CREATION OF SEMICONDUCTOR MULTI-SLOPED FEATURES

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APPEAL BRIEF

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Dear Sir:

Applicant submits this brief in connection with an appeal of the above-identified patent application. A credit card payment form is filed concurrently herewith in connection with all fees due regarding this appeal brief. In the event any additional fees may be due and/or are not covered by the credit card, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1063 [AMDP660US].

I. Real Party in Interest (37 C.F.R. §41.37(c)(1)(i))

The real party in interest in the present appeal is Advanced Micro Devices, Inc., the assignee of the present application.

II. Related Appeals and Interferences (37 C.F.R. §41.37(c)(1)(ii))

Appellants, appellants' legal representative, and/or the assignee of the present application are not aware of any appeals or interferences which may be related to, will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims (37 C.F.R. §41.37(c)(1)(iii))

Claim 30 has been withdrawn, and no claims have been cancelled or allowed. Claims 1-29 stand rejected by the Examiner. The rejection of claims 1-29 is being appealed.

IV. Status of Amendments (37 C.F.R. §41.37(c)(1)(iv))

No claim amendments have been entered after the Final Office Action.

V. Summary of Claimed Subject Matter (37 C.F.R. §41.37(c)(1)(v))

Independent claim 1

Independent claim 1 recites a system for *in-situ* regulation of an etch process employed in fabricating a multi-sloped semiconductor feature on a wafer, comprising one or more etching components operative to etch at least one aspect of a multi-sloped feature on a wafer; an etch component controller for controlling the one or more etching components; a system for directing light onto the wafer; a measuring system for measuring at least one etching parameter based on light reflected from the wafer; and a process analyzer operatively coupled to the measuring system and the etch component controller, wherein the process analyzer receives the measured parameters from the measuring system and analyzes the measured parameters to determine whether adjustments to the etching components are needed to fabricate the multi-sloped features within desired critical dimension tolerances and where the process analyzer stores the measured parameters to facilitate reproducing process conditions. (*See e.g.* page 10 line 17 – page 12 line 8 and Figure 8).

Independent claim 8

Independent claim 8 recites a method for *in-situ* regulation of a process for etching a multi-sloped semiconductor device formed on a wafer, comprising partitioning the wafer into one or more portions; etching at least one multi-sloped device on at least one portion of the wafer; directing light onto at least one portion of the wafer; collecting light reflected from the at least one portion; analyzing the reflected light to determine the acceptability of the multi-sloped semiconductor device on the at least one portion; storing data associated with the acceptability of the multi-sloped semiconductor device and one or more processing conditions associated with creating the multi-sloped semiconductor device to facilitate reproducing the one or more processing conditions; and selectively controlling one or more etching components to regulate the etching of the multi-sloped semiconductor device on the at least one portion. (*See e.g.* page 15 line 26 – page 17 line 5 and figure 14).

Independent claim 12

Independent claim 12 recites a method for *in-situ* regulation of an etch process of a multi-sloped semiconductor device formed on a wafer, comprising partitioning the wafer into a plurality of grid blocks; using one or more etching components to etch a multi-sloped semiconductor feature on the wafer, each etching component functionally corresponding to a respective grid block; measuring at least one etch parameter associated with the multi-sloped semiconductor feature; determining etching conditions at the at least one grid block according to the measured etch parameter; and using a process analyzer to selectively control the plurality of etching components to compensate for wafer to wafer variations during the etch process of the multi-sloped feature. (*See e.g.* page 15 line 26 – page 17 line 5 and figure 14).

Independent claim 13

Independent claim 13 recites a system for *in-situ* regulation of an etch process of a multi-sloped semiconductor device formed on a wafer, comprising means for partitioning the wafer into a plurality of portions (*See e.g.* page 15 lines 31–33 and figure 14); means for etching at least one multi-sloped device on at least one portion of the wafer (*See e.g.* page 13 lines 27-29 and Figure 10); means for directing light onto at least one portion of the wafer (*See e.g.* page 15 lines 1-5 and Figure 13); means for collecting light reflected from the at least one portion (*See*

e.g. page 15 lines 1-14 and Figure 13)); means for analyzing the reflected light to determine the acceptability of the etching of the at least one portion (*See e.g.* page 15 line 26 – page 16 line 29 and Figure 14); and means for selectively controlling one or more etching components to regulate the etching of the multi-sloped semiconductor device on the at least one portion (*See e.g.* page 17 lines 1-5 and Figure 14).

Independent claim 14

Independent claim 14 recites a data packet adapted to be transmitted between two or more processes, the data packet containing information related to *in-situ* adaptation of an etch process employed in fabricating a multi-sloped semiconductor device, where the information was generated by a system for *in-situ* regulation of an etch process employed in fabricating a multi-sloped semiconductor feature on a wafer, the system comprising one or more etching components operative to etch at least one aspect of a multi-sloped feature on a wafer; an etch component controller for controlling the one or more etching components; a system for directing light onto the wafer; a measuring system for measuring at least one etching parameter based on light reflected from the wafer; and a process analyzer operatively coupled to the measuring system and the etch component controller, wherein the process analyzer receives the measured parameters from the measuring system and analyzes the measured parameters to determine whether adjustments to the etching components are needed to fabricate the multi-sloped features within desired critical dimension tolerances and where the process analyzer stores the measured parameters to facilitate reproducing process conditions. (*See e.g.* page 10 line 17 – page 12 line 8 and Figure 8).

Independent claim 15

Independent claim 15 recites a method employed for manufacturing semiconductor devices, comprising determining a desired multi-sloped profile; etching at least one device to conform to the desired multi-sloped profile; detecting *in situ* parameters of the etching of the device utilizing scatterometry; and adjusting the etching of the multi-sloped profile as necessary to produce the desired multi-sloped profile. (*See e.g.* page 17 lines 7 – 24 and Figure 15).

Independent claim 25

Independent claim 25 recites a semiconductor device manufacturing system, comprising at least one etch component for etching a device to conform to a desired multi-sloped profile; a detecting system employing scatterometry for detecting *in situ* parameters related to the etching of the device; and an etch component controller capable of receiving information from the detecting system to control the etch component as necessary to produce the desired multi-sloped profile. (*See e.g.* page 13 line 30 – page 14 line 13 and Figure 11).

Independent claim 29

Independent claim 29 recites a system for manufacturing semiconductor devices, comprising means for etching at least one device to conform to a desired multi-sloped profile (*See e.g.* page 15 line 31 – page 16 line 1 and Figure 14); means for detecting *in situ* parameters of the etching of the device utilizing scatterometry (*See e.g.* page 17 lines 7 – 16 and Figure 15); and means for adjusting the etching of the multi-sloped profile as necessary to produce the desired multi-sloped profile (*See e.g.* page 17 lines 16 – 24 and Figure 15).

VI. Grounds of Rejection to be Reviewed (37 C.F.R. §41.37(c)(1)(vi))

A. Whether claims 1-29 are unpatentable under 35 U.S.C. §103(a) over Miller *et al.* (US 6,643,557), in view of the acknowledged prior art and Moslehi (US 5,719,495).

VII. Argument (37 C.F.R. §41.37(c)(1)(vii))

A. Rejection of Claims 1-29 Under 35 U.S.C. §103(a)

Claims 1-29 stand rejected as obvious under 35 U.S.C. §103(a) over Miller *et al.* (US 6,643,557), in view of the acknowledged prior art and Moslehi (US 5,719,495). Applicants' representative respectfully requests that this rejection be withdrawn for at least the following reasons. The cited references, either alone or in combination, fail to disclose or suggest all limitations of the subject claims.

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) ***must teach or suggest all the claim limitations.*** *See* MPEP §706.02(j). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must be found in the prior art and not based on the Applicant's disclosure. *See In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added).

The claimed invention relates to a system for regulating an etch process for the fabrication of multi-sloped semiconductor features. In particular, independent claims 1, 8, 12-15, 25 and 29 recite similar limitations, namely ***a system for in-situ regulation of an etch process employed in fabricating multi-sloped semiconductor features on a wafer comprising one or more etching components operative to etch at least one aspect of a multi-sloped feature on a wafer*** and ***an etch component controller for controlling one or more etching components.*** Miller *et al.*, Moslehi and the acknowledged art, either alone or in combination, fails to disclose or suggest such novel features of applicants' claimed invention.

Moslehi relates to a system for *in-situ* monitoring of physical properties of metal and other material layers as well as semiconductor wafer surface roughness. On page 3 of the Final Office Action (dated March 24, 2005), it is erroneously asserted that Moslehi shows the *in-situ* use of an optical measurement device for *process control in processing tools* such as etch processes. This contention is supported by a portion of Moslehi that shows the use of "critical *in-situ* sensors (real-time as well as pre and post-process sensors) for...anisotropic plasma etch...and isotropic plasma etch." *See* col. 8, lines 20-27. Thus, Moslehi provides for rudimentary *in-situ monitoring* of etch processes, but nowhere does the cited document teach or suggest ***in-situ regulation*** of an etch process, as claimed. Instead, Moslehi is limited to allowing for real-time chemical and physical vapor control. *See* col. 8, line 65 – col. 9 line 13. Consequently, the reference is silent with regard to the claimed limitations of ***in-situ regulation of an etch process...comprising one or more etching components operative to etch at least one***

aspect of a multi-sloped feature on a wafer and ***an etch component controller for controlling the one or more etching components.***

Furthermore, neither Miller *et al.* nor the portion of the instant specification indicated by the Examiner as acknowledged prior art compensate for the deficiencies of Moslehi. Miller *et al.* is directed towards utilizing scatterometry to measure non-slope semiconductor features, and as conceded by the Examiner, the reference does not make measurements *in-situ.* In addition, at the portions indicated by the Examiner, the instant specification recognizes that any scatterometry system known in the art can be used as a measuring system to practice the subject invention. Nowhere is it mentioned that it is known in the art to regulate etch processes *in-situ* for multi-slope semiconductor features on a wafer, and therefore, the acknowledged prior art does not make up for the shortcomings of Moslehi.

The Federal Circuit has consistently held that in order to establish obviousness *vis-à-vis* a combination of cited references, the cited references ***must themselves provide a suggestion for the combination*** to one of ordinary skill in the art. The suggestion for such a combination cannot and must not be based on applicants' disclosure using hindsight. *See In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Here, neither the nature of the problem to be solved, the teachings in the cited art, nor the knowledge of persons of ordinary skill provides sufficient suggestion or motivation to combine the references. Instead, the Examiner relies on improper hindsight in reaching his obviousness determination. The Federal Court has held that to imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the invention taught is used against its teacher. ***One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to depreciate the claimed invention.*** *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d (BNA) 1596 (Fed. Cir. 1988) (citations omitted and emphasis added).

In view of at least the foregoing, it is readily apparent that the cited references, either alone or in combination, fail to teach or suggest all limitations of independent claims 1, 8, 12-15, 25 and 29 (and the claims that depend there from). Accordingly, withdrawal of this rejection is respectfully requested.

B. Conclusion

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited references. Accordingly, it is respectfully requested that the rejections of claims 1-29 be reversed.

If any additional fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [AMDP660US].

Respectfully submitted,
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VIII. Claims Appendix (37 C.F.R. §41.37(c)(1)(viii))

1. A system for *in-situ* regulation of an etch process employed in fabricating a multi-sloped semiconductor feature on a wafer, comprising:

one or more etching components operative to etch at least one aspect of a multi-sloped feature on a wafer;

an etch component controller for controlling the one or more etching components;

a system for directing light onto the wafer;

a measuring system for measuring at least one etching parameter based on light reflected from the wafer; and

a process analyzer operatively coupled to the measuring system and the etch component controller, wherein the process analyzer receives the measured parameters from the measuring system and analyzes the measured parameters to determine whether adjustments to the etching components are needed to fabricate the multi-sloped features within desired critical dimension tolerances and where the process analyzer stores the measured parameters to facilitate reproducing process conditions.

2. The system of claim 1, the measuring system further including a scatterometry system for collecting the reflected light, wherein the measuring system interprets the reflected light to produce the measured etch parameters using scatterometry techniques.

3. The system of claim 2, wherein the measured etch parameters include at least one of feature height, feature width, slope of one or more feature sides and angles between feature sides.

4. The system of claim 3, wherein the multi-sloped feature has one or more angles between feature sides that are not right angles.

5. The system of claim 2, wherein the process analyzer:

partitions the wafer into a plurality of grid blocks; and

determines whether to make adjustments to one or more etching components associated with one or more grid blocks by analyzing measured etch parameters corresponding to one or more grid blocks.

6. The system of claim 5, wherein the process analyzer determines that adjustments to one or more etching components are necessary for at least a portion of the wafer by comparing one or more measured etch parameter values to one or more stored acceptable etch parameter values.

7. The system of claim 6, wherein the stored acceptable etch parameter values are stored as scatterometry signatures.

8. A method for *in-situ* regulation of a process for etching a multi-sloped semiconductor device formed on a wafer, comprising:

partitioning the wafer into one or more portions;

etching at least one multi-sloped device on at least one portion of the wafer;

directing light onto at least one portion of the wafer;

collecting light reflected from the at least one portion;

analyzing the reflected light to determine the acceptability of the multi-sloped semiconductor device on the at least one portion;

storing data associated with the acceptability of the multi-sloped semiconductor device and one or more processing conditions associated with creating the multi-sloped semiconductor device to facilitate reproducing the one or more processing conditions; and

selectively controlling one or more etching components to regulate the etching of the multi-sloped semiconductor device on the at least one portion.

9. The method of claim 8, wherein the light is collected by a scatterometry measuring system.

10. The method of claim 9. wherein the scatterometry measuring system interprets the reflected light into measured etch parameters associated with the at least one portion using scatterometry techniques.

11. The method of claim 10, wherein the measured etch parameters are compared to stored acceptable etch parameter values in order to determine whether one or more adjustments to the process for etching a multi-sloped semiconductor device formed on a wafer is necessary.

12. A method for *in-situ* regulation of an etch process of a multi-sloped semiconductor device formed on a wafer, comprising:

partitioning the wafer into a plurality of grid blocks;

using one or more etching components to etch a multi-sloped semiconductor feature on the wafer, each etching component functionally corresponding to a respective grid block;

measuring at least one etch parameter associated with the multi-sloped semiconductor feature;

determining etching conditions at the at least one grid block according to the measured etch parameter; and

using a process analyzer to selectively control the plurality of etching components to compensate for wafer to wafer variations during the etch process of the multi-sloped feature.

13. A system for *in-situ* regulation of an etch process of a multi-sloped semiconductor device formed on a wafer, comprising:

means for partitioning the wafer into a plurality of portions;

means for etching at least one multi-sloped device on at least one portion of the wafer;

means for directing light onto at least one portion of the wafer;

means for collecting light reflected from the at least one portion;

means for analyzing the reflected light to determine the acceptability of the etching of the at least one portion; and

means for selectively controlling one or more etching components to regulate the etching of the multi-sloped semiconductor device on the at least one portion.

14. A data packet adapted to be transmitted between two or more processes, the data packet containing information related to *in-situ* adaptation of an etch process employed in fabricating a multi-sloped semiconductor device, where the information was generated by a system for *in-situ* regulation of an etch process employed in fabricating a multi-sloped semiconductor feature on a wafer, the system comprising:

one or more etching components operative to etch at least one aspect of a multi-sloped feature on a wafer;

an etch component controller for controlling the one or more etching components;

a system for directing light onto the wafer;

a measuring system for measuring at least one etching parameter based on light reflected from the wafer; and

a process analyzer operatively coupled to the measuring system and the etch component controller, wherein the process analyzer receives the measured parameters from the measuring system and analyzes the measured parameters to determine whether adjustments to the etching components are needed to fabricate the multi-sloped features within desired critical dimension tolerances and where the process analyzer stores the measured parameters to facilitate reproducing process conditions.

15. A method employed for manufacturing semiconductor devices, comprising:

determining a desired multi-sloped profile;

etching at least one device to conform to the desired multi-sloped profile;

detecting *in situ* parameters of the etching of the device utilizing scatterometry; and

adjusting the etching of the multi-sloped profile as necessary to produce the desired multi-sloped profile.

16. The method of claim 15, further including storing the desired multi-sloped profile.

17. The method of claim 15, further including analyzing the parameters of the etching of the device.

18. The method of claim 17, wherein analyzing includes comparing current parameters to previous parameters.

19. The method of claim 15, further including storing the parameters found while detecting *in situ* parameters.

20. The method of claim 15, wherein adjusting the etching of the multi-sloped profile includes at least one from a group consisting of reducing a rate of etching and increasing a rate of etching.

21. The method of claim 15, further including controlling light sources utilized in detecting *in situ* parameters.

22. The method of claim 21, wherein controlling light sources includes at least one from a group consisting of reducing a light source intensity, increasing a light source intensity and altering an angle of a light source.

23. The method of claim 15, further including controlling light receivers utilized in detecting *in situ* parameters.

24. The method of claim 23, wherein controlling light receivers includes at least one from a group consisting of reducing a light receiver sensitivity, increasing a light receiver sensitivity and altering an angle of a light receiver.

25. A semiconductor device manufacturing system, comprising:

at least one etch component for etching a device to conform to a desired multi-sloped profile;

a detecting system employing scatterometry for detecting *in situ* parameters related to the etching of the device; and

an etch component controller capable of receiving information from the detecting system to control the etch component as necessary to produce the desired multi-sloped profile.

26. The system of claim 25, further comprising an analysis system to analyze *in situ* parameters provided by the detecting system.

27. The system of claim 26, the analysis system additionally analyzes *in situ* parameters based on at least one from a group consisting of current *in situ* parameters, previous *in situ* parameters, scatterometry signature profiles, and predetermined multi-sloped profiles.

28. The system of claim 25, further comprising a storage medium for storing at least one from a group consisting of current *in situ* parameters, previous *in situ* parameters, scatterometry signature profiles, and predetermined multi-sloped profiles.

29. A system for manufacturing semiconductor devices, comprising:

means for etching at least one device to conform to a desired multi-sloped profile;

means for detecting *in situ* parameters of the etching of the device utilizing scatterometry; and

means for adjusting the etching of the multi-sloped profile as necessary to produce the desired multi-sloped profile.

30. (Withdrawn) A data packet transmitted between two or more components that facilitates semiconductor device manufacture, the data packet comprising information, based, in part, on a scatterometry derived means for producing multi-sloped profiled devices.

IX. Evidence Appendix (37 C.F.R. §41.37(c)(1)(ix))

None.

X. Related Proceedings Appendix (37 C.F.R. §41.37(c)(1)(x))

None.